

## METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

### Field of the Invention

5       The present invention relates to a method for fabricating a semiconductor device; and, more particularly, to a method for fabricating a semiconductor device capable of preventing diffusions of a wet solution used in a wet etching process into an unintended region.

### Description of Related Arts

10       As an integration level of a semiconductor device has been highly progressed, it is difficult to secure process margins. To solve this problem, a self-aligned contact (SAC) process is adopted for forming a contact in a cell region. However, a bottom side area of the contact inevitably decreases while an aspect ratio increases as the integration level increases. This increase of the aspect ratio causes the  
20   contact area to be decreased in more extents.

      Therefore, a wet etching process is employed after the contact is formed in the cell region through the use of the typical SAC process in order to secure a maximal area of an opened portion of the contact. However, this wet etching  
25   process etches partially an insulation layer usually made of boron-phosphorus-silicate glass (BPSG).

      Figs. 1A and 1B are top views of a conventional

semiconductor device before and after a wet cleaning/etching process for extending an opened portion of a contact after the typical SAC process is performed.

Prior to performing the wet etching process, a plurality  
5 of contact holes 120 are formed between conductive patterns 110. A plurality of insulating patterns 100 are formed adjacent to the contact holes 120 in a direction of crossing the conductive patterns 110. Herein, the conductive pattern 110 can be a gate electrode pattern, a bit line pattern or a  
10 metal wire. Also, the conductive pattern 110 is a line-type conductive pattern.

At this time, the wet etching process usually uses hydrofluoric acid (HF)-based solutions with a consideration of an etch characteristic of the oxide-based insulating pattern  
15 100. However, this use of the HF-based solution results in a corrosion of the insulating pattern 100, thereby degrading overall insulating characteristics of the semiconductor device.

In case of fabricating a dynamic random access memory (DRAM) device, a contact hole is formed in a cell region and a  
20 plug being electrically connected to a source/drain region through the contact hole is formed by using a selective epitaxial growth (SEG) technique or a deposition technique. Afterwards, a post landing plug source drain (PLSD) process is performed in a peripheral circuit region.

25 However, because of a recent trend in large-scale integration of the semiconductor device, the SEG technique is used in forming the plug instead of a polysilicon deposition

in order to decrease a cell contact resistance. In case of the SEG technique, a temperature for carrying out the plug formation process ranges from about 700 °C to about 1000 °C. This temperature range is higher than that of the polysilicon deposition process typically ranging from about 500 °C to about 600°C. Therefore, this SEG technique degrades electrical properties such as a threshold voltage  $V_t$ , a drain current  $I_d$  and a punchthrough phenomenon in the peripheral circuit region.

For this reason, source/drains are formed at both sides of a gate electrode structure in the peripheral circuit region after a contact pad is formed in the cell region through the use of the SEG technique to prevent degradation of electrical properties.

Fig. 2 is a top view showing the conventional semiconductor device after completion of the typical SAC process for forming a plug. As shown, a plurality of insulating patterns 25 are locally arrayed on a substrate 20 in which active regions are formed. A plurality of gate electrodes G1 and G2 are arrayed in a direction of crossing the insulating patterns 25. Herein, the reference numeral 27 is a region opened for forming a plug, i.e., a contact hole, and the X-X' and Y-Y' regions are a cell region and a peripheral circuit region, respectively.

Figs. 3A to 3D are cross-sectional views of a conventionally fabricated semiconductor device in each direction of the lines A-A' and B-B' shown in Fig. 2.

Referring to Fig. 3A, an insulation layer 21 for forming a gate electrode (hereinafter referred to as gate insulation layer), a conductive layer 22 for forming a gate electrode (hereinafter referred to as gate conductive layer) and an  
5 insulation layer 23 for a hard mask (hereinafter referred to as hard mask insulation layer) are sequentially deposited on a substrate providing various elements of the semiconductor device. Then, a photo-etching process is performed with use of a gate electrode mask to form a plurality of gate  
10 electrodes G1 and G2 having a stack structure of the hard mask insulation layer 23, the gate conductive layer 22 and the gate insulation layer 21.

Herein, the gate insulation layer 21 is an oxide-based layer. The gate conductive layer 22 is a single layer or  
15 stacked layer of tungsten, tungsten nitride, or tungsten silicide. Also, the hard mask insulation layer 23 is a nitride-based layer using a silicon nitride layer or a silicon oxynitride layer.

The reason for using the nitride-based material for the  
20 hard mask insulation layer 23 is to provide an intended etch profile in the SAC process for forming the plug and simultaneously to prevent losses of the gate electrode patterns G1 and G2 because the nitride-based material has a different etch selectivity from an oxide-based inter-layer  
25 insulation layer.

Next, a nitride-based etch stop layer 24 is deposited thinly along a profile containing the gate electrode patterns

G1 and G2. An oxide-based insulation layer 25 for insulating inter-layers and isolating the gate electrode patterns G1 and G2 from each other is deposited on an entire surface of the above substrate structure. At this time, the insulation layer  
5 25 is made of boron-phosphorus silicate glass (BPSG).

Referring to Fig. 3B, subsequent to the deposition of the insulation layer 25, a photoresist pattern 26, which is a cell contact open mask, is formed on the insulation layer 25. The insulation layer 25 is then selectively etched by using  
10 the photoresist pattern 26 as an etch mask to form a plurality of contact holes 27 exposing impurity contact regions, e.g., source/drains, allocated between the gate electrode patterns G1 in the cell region X-X'. The contact holes 27 in the cell region X-X' viewed in a direction of the line B-B' exposes  
15 impurity contact regions allocated between the insulating patterns, i.e., the etched insulation layers 25.

A photoresist strip process is performed to remove the photoresist pattern 26, and a cleaning process using a HF-based solution is subsequently performed to remove etch  
20 remnants and extend an opened portion of the contact hole 27.

A conductive layer for forming a plug (hereinafter referred to as plug conductive layer) is deposited into the contact holes 27 so as to be electrically connected to an exposed surface of the substrate 20 during the contact hole  
25 formation. The plug conductive layer is made of polysilicon or tungsten, and a barrier layer using Ti/TiN can be formed at a bottom of the plug conductive layer.

Referring to Fig. 3C, after depositing the plug  
conductive layer, a chemical mechanical polishing (CMP)  
process is performed under a target that the insulation layer  
25 remains on an upper part of each gate electrode pattern G1  
5 and G2 with a certain thickness. Thereafter, a plurality of  
plugs 28 isolated from each other by the remaining insulation  
layer 25 are formed.

As shown in Fig. 3D, the insulation layer 25 formed in  
the peripheral circuit region Y-Y' is removed through the use  
10 of a wet etching process. More specifically, a photoresist  
pattern 29 masking solely an upper part of the cell region X-  
X' is formed. Then, the insulation layer 25 formed in the  
peripheral circuit region Y-Y' is selectively removed by using  
buffered oxide etchant (BOE) or hydrofluoric acid (HF).

15 During the wet etching process, the above wet solution  
is, however, diffused into the cell region X-X'. This  
diffusion is denoted as the reference numeral 31. As a result  
of this diffusion, the insulation layer 25 in the cell region  
X-X' is excessively etched to thereby expose the plugs 28.  
20 This exposure is denoted as the reference numeral 32.  
Particularly, in case that the insulation layer 25 is made of  
BPSG, the BPSG has a poor adhesion with the photoresist.  
Therefore, the wet solution is diffused through interstitial  
spaces between the BPSG layer, i.e., the insulation layer 25,  
25 and the photoresist pattern 29, further resulting in  
generations of void 30. Furthermore, the void 30 becomes a  
factor for inducing an electrical short circuit between bit

lines during a SAC process for forming a bit line contact because a polishing agent for the CMP process for isolating cells is filled into the voids 30.

## 5 Summary of the Invention

It is, therefore, an object of the present invention to provide a method for fabricating a semiconductor device capable of efficiently preventing defects in a semiconductor  
10 device caused by diffusions of a wet solution into a cell region during a removal of an insulation layer in a peripheral circuit region.

In accordance with an aspect of the present invention, there is provided a method for fabricating a semiconductor  
15 device, including the steps of: (a) forming a plurality of conductive patterns on a substrate in a cell region and a peripheral circuit region; (b) forming an insulation layer on an entire surface of the resulting structure from the step (a); (c) forming a plurality of plugs in the cell region and  
20 simultaneously forming a dummy pattern in a region between the cell region and the peripheral circuit region, each plug and the dummy pattern being contacted to the substrate allocated between the conductive patterns by passing through the insulation layer; (d) forming a photoresist pattern masking  
25 the resulting structure in the cell region; and (e) removing the insulation layer in the peripheral circuit region by performing a wet etching process with use of the photoresist

pattern as an etch mask to thereby expose a surface of the substrate in the peripheral circuit region.

In accordance with another aspect of the present invention, there is also provided a method for fabricating a semiconductor device, including the steps of: (a) forming a plurality of conductive patterns on a substrate in a cell region and a peripheral circuit region; (b) forming an insulation layer on an entire surface of the resulting structure from the step (a); (c) forming a plurality of plugs in the cell region, each being contacted to the substrate allocated between the conductive patterns by passing through the insulation layer; (d) forming a photoresist pattern masking the resulting structure in the cell region; (e) performing a dry etching process with use of the photoresist pattern as an etch mask to remove partially the insulation layer in the peripheral circuit region; and (f) removing the remaining insulation layer through a wet etching process to thereby expose a surface of the substrate in the peripheral circuit region.

In accordance with still another aspect of the present invention, there is also provided a method for fabricating a semiconductor device, including the steps of: (a) forming a plurality of conductive patterns on a substrate in a cell region and a peripheral circuit region; (b) forming a planarized first insulation layer on an entire surface of the resulting structure from the step (a); (c) forming a second insulation layer on the first insulation layer; (d) forming a



plurality of plugs in the cell region, each being contacted to the substrate allocated between the conductive patterns by passing through the first and the second insulation layers; (e) forming a photoresist pattern masking the resulting structure in the cell region; and (f) performing a wet etching process with use of the photoresist pattern as an etch mask to remove the first and the second insulation layers disposed in the peripheral circuit region.

10 Brief Description of the Drawing(s)

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

Figs. 1A and 1B are top views of a conventional semiconductor device before and after a wet cleaning/etching process for extending an opened portion of a contact hole;

Fig. 2 is a top view of the conventional semiconductor device after a SAC process for forming a plug;

Figs. 3A to 3D are cross-sectional views of the semiconductor device viewed in each direction of the lines A-A' and B-B' shown in Fig. 1A;

Figs. 4A to 4D are cross-sectional views of a semiconductor device in each direction of the lines A-A' and B-B' shown like Fig. 1A in accordance with a first preferred embodiment of the present invention;

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Figs. 5A to 5E are cross-sectional views of a semiconductor device in each direction of the lines A-A' and B-B' shown like in Fig. 1A in accordance with a second preferred embodiment of the present invention; and

5 Figs. 6A to 6D are cross-sectional views of a semiconductor device in each direction of the lines A-A' and B-B' shown like Fig. 1 in accordance with a third preferred embodiment of the present invention.

10 Detailed Description of the Invention

Hereinafter, a method for fabricating a semiconductor device capable of preventing defects in a semiconductor device will be described in the following.

15 Figs. 4A to 4D are cross-sectional views of a semiconductor device in each direction of the lines A-A' and B-B' shown like Fig. 1A in accordance with a first preferred embodiment of the present invention.

Referring to Fig. 4A, an insulation layer 41 for forming  
20 a gate electrode (hereinafter referred to as gate insulation layer), a conductive layer 42 for forming a gate electrode (hereinafter referred to as gate conductive layer) and an insulation layer for forming a hard mask (hereinafter referred to as hard mask insulation layer) are sequentially deposited  
25 on a substrate 40 providing various elements of a semiconductor device. Afterwards, a photo-etching process is performed by using a gate electrode mask in order to form a

plurality of gate electrodes G1 and G2 having a stack structure of the hard mask insulation layer 43, the gate conductive layer 42 and the gate insulation layer 41.

At this time, the gate insulation layer 41 is an oxide-based layer. The gate conductive layer 42 is a single layer or stack layer of tungsten, tungsten nitride or tungsten silicide. Also, the hard mask insulation layer 43 is a nitride-based layer such as a silicon nitride layer or a silicon oxynitride layer.

The reason for using the nitride-based material for the hard mask insulation layer 43 is to provide an intended etch profile in the SAC process for forming the plug and simultaneously to prevent losses of the gate electrode patterns G1 and G2 because the nitride-based material has a different etch selectivity from an oxide-based inter-layer insulation layer.

Next, a nitride-based etch stop layer 44 is deposited thinly along a profile containing the gate electrode patterns G1 and G2. An oxide-based insulation layer 45 for insulating inter-layers and isolating the gate electrode patterns G1 and G2 from each other is deposited on an entire surface of the above substrate structure. At this time, the insulation layer 45 is a single layer or stacked layer of boron-phosphorus silicate glass (BPSG), tetra-ethyl-ortho silicate (TEOS) or high density plasma (HDP) oxide. Herein, the region C-C' allocated between the cell region X-X' and the peripheral circuit region Y-Y' is designated for a dummy pattern region.

Referring to Fig. 4B, subsequent to the insulation layer 45 deposition, a photoresist pattern 46, which is a cell contact open mask, is formed on the insulation layer 45. Then, the insulation layer 45 viewed in a direction of the line A-A' is selectively etched with use of the photoresist pattern 46 as an etch mask so that a plurality of opening parts 47 exposing substrate regions, e.g., impurity contact regions such like source/drains disposed between the gate electrode patterns G1 and G2 are formed in the cell region X-X'. On the other hand, the opening parts 47 viewed in a direction of the line B-B' expose the substrate region disposed between the insulating patterns, i.e., the etched insulation layer 45. Also, an opening part 47' exposing a surface of the substrate 40 is formed in the region C-C' designated for the dummy patterns. Hereinafter, the region C-C' is referred to as dummy pattern region.

Next, a photoresist strip process is carried out to remove the photoresist pattern 46, and then, a cleaning process is performed to remove etch remnants and extend a bottom portion of the opening parts 47 and 47'.

Referring to Fig. 4C, a conductive layer for forming a plug (hereinafter referred to as plug conductive layer) is deposited on the above entire structure so as to be electrically connected to the exposed substrate 40. Afterwards, a CMP process is performed in such a manner that the insulation layer 45 remains on an upper part of the gate electrode patterns G1 and G2 with a certain thickness. From

this CMP process, a plurality of plugs 48 and 48' isolated from each other by the insulation layer 45 are formed. The plug conductive layer is made of polysilicon or tungsten, and a barrier layer such as Ti/TiN can be formed at a bottom of the plug conductive layer. It is possible to employ a selective epitaxial growth (SEG) technique for forming the plug conductive layer instead of using the above-described deposition technique.

It is also noted that the plug 48' is formed in the dummy pattern region C-C'. Unlike the plugs 48 formed in the cell region X-X' for making an electrical connection with the impurity contact regions, the plug 48' is for preventing diffusions of a wet solution into the cell region X-X' when the insulation layer 45 in the peripheral circuit region Y-Y' is removed during a subsequent post landing plug source drain (PLSD) process. At this time, the dummy pattern region C-C' has preferably a width ranging from about 1  $\mu\text{m}$  to about 10  $\mu\text{m}$ .

Next, referring to Fig. 4D, the insulation layer 45 in the peripheral circuit region Y-Y' is removed through the use of a wet etching process. This removal of the insulation layer 45 is denoted as the reference numeral 50. In more detail, a photoresist pattern 49 masking an upper part of the cell region X-X' is formed, and the insulation layer 45 in the peripheral circuit region Y-Y' is removed thereafter.

At this time, the wet etching process uses a wet solution such as buffered oxide etchant (BOE) or hydrofluoric acid (HF). As mentioned above, the plug 48' has a function of

preventing diffusions of the wet solution into the cell region X-X' during the wet etching process. Hereinafter, the plug 48' is referred to as a dummy plug. Also, the wet solution is mainly used for etching an oxide layer. Therefore, even if  
5 the dummy plug 48' is slightly attacked by the diffused wet solution, it is still possible to prevent the diffusion of the wet solution into the cell region X-X'. Also, since the attacked plug 48' is the dummy plug, it does not affect device characteristics.

10 Figs. 5A to 5E are cross-sectional views of a semiconductor device viewed in each direction of the lines A-A' and B-B' shown like in Fig. 1A in accordance with a second preferred embodiment of the present invention.

Referring to Fig. 5A, a gate insulation layer 61, a gate  
15 conductive layer 62 and a hard mask insulation layer 63 are sequentially deposited on a substrate 60 providing various elements of a semiconductor device. Afterwards, a photo-etching process is performed by using a gate electrode mask in order to form a plurality of gate electrodes G1 and G2 having  
20 a stack structure of the hard mask insulation layer 63, the gate conductive layer 62 and the gate insulation layer 61.

At this time, the gate insulation layer 61 is an oxide-based layer. The gate conductive layer 62 is a single layer or stack layer of tungsten, tungsten nitride or tungsten  
25 silicide. Also, the hard mask insulation layer 63 is a nitride-based layer such as a silicon nitride layer or a silicon oxynitride layer.

The reason for using the nitride-based material for the hard mask insulation layer 63 is to provide an intended etch profile in the SAC process for forming the plug and simultaneously to prevent losses of the gate electrode patterns G1 and G2 because the nitride-based material has a different etch selectivity from an oxide-based inter-layer insulation layer.

Next, a nitride-based etch stop layer 64 is deposited thinly along a profile containing the gate electrode patterns G1 and G2. An oxide-based insulation layer 65 for insulating inter-layers and isolating the gate electrode patterns G1 and G2 from each other is deposited on an entire surface of the above substrate structure. At this time, the insulation layer 65 is a single layer or stacked layer of BPSG, boron-silicate glass (BSG), phosphorus-silicate glass (PSG), TEOS, HDP oxide or an advanced planarization layer (APL).

Referring to Fig. 5B, subsequent to the insulation layer 65 deposition, a photoresist pattern 66, which is a cell contact open mask, is formed on the insulation layer 65. Then, the insulation layer 65 viewed in a direction of the line A-A' is selectively etched with use of the photoresist pattern 66 as an etch mask so that a plurality of opening parts 67 exposing substrate regions, e.g., impurity contact regions such like source/drains disposed between the gate electrode patterns G1 are formed in the cell region X-X'. On the other hand, the opening parts 67 viewed in a direction of the line B-B' expose the substrate region disposed between the

insulating patterns, i.e., the etched insulation layer 65.

Next, a photoresist strip process is carried out to remove the photoresist pattern 66, and then, a cleaning process is performed to remove etch remnants.

5 Referring to Fig. 5C, a plug conductive layer is deposited on the above entire structure so as to be electrically connected to the exposed substrate 60. Herein, the plug conductive layer is made of polysilicon or tungsten, and a barrier layer such as Ti/TiN can be formed at a bottom  
10 of the plug conductive layer. Afterwards, a CMP process is performed in such a manner that the insulation layer 65 remains on an upper part of the gate electrode patterns G1 and G2 with a certain thickness. From this CMP process, a plurality of plugs 68 isolated from each other by the  
15 insulation layer 65 are formed.

Next, referring to Fig. 5D, a partial portion of the insulation layer 45 in the peripheral circuit region Y-Y' is removed through the use of a dry etching process. This partial removal of the insulation layer 65 is denoted as the  
20 reference numeral 70. In more detail, a photoresist pattern 69 masking an upper part of the cell region X-X' is formed, and the insulation layer 65 in the peripheral circuit region Y-Y' is selectively removed by using the photoresist pattern 69 as an etch mask. Herein, for the dry etching process, a  
25 plasma using a mixed gas of  $C_xF_y$ , where x and y ranges from about 1 to about 10,  $C_aH_bF_c$ , where a, b and c ranges from about 1 to about 10, and  $O_2$  is used. At this time, such inert gas



as He, Ne, Ar or Xe can be used additionally to enhance reliability of an etch profile. Also, the reference numeral 64' illustrates that the etch stop layer 64 is partially etched during the dry etching process.

5 Referring to Fig. 5E, the dry etching process, a wet etching process is performed to remove the remaining insulation layer 65 in the peripheral circuit region Y-Y'. This removal is denoted as the reference numeral 71. At this time, such wet solution as BOE or HF is used in the wet  
10 etching process.

By performing the dry etching process having an anisotropic etching property prior to the wet etching process, it is possible to shorten a period for performing the wet etching process. This effect further prevents diffusions of  
15 the wet solution into the cell region X-X' through the insulation layer 65.

Figs. 6A to 6D are cross-sectional views of a semiconductor device in each direction of the lines A-A' and B-B' shown like in Fig. 1A in accordance with a third  
20 preferred embodiment of the present invention.

Referring to Fig. 6A, a gate insulation layer 81, a gate conductive layer 82 and a hard mask insulation layer 83 are sequentially deposited on a substrate 80 providing various elements of a semiconductor device. Afterwards, a photo-  
25 etching process is performed by using a gate electrode mask in order to form a plurality of gate electrodes G1 and G2 having a stack structure of the hard mask insulation layer 83, the

gate conductive layer 82 and the gate insulation layer 81.

At this time, the gate insulation layer 81 is an oxide-based layer. The gate conductive layer 82 is a single layer or stack layer of tungsten, tungsten nitride or tungsten silicide. Also, the hard mask insulation layer 83 is a nitride-based layer such as a silicon nitride layer or a silicon oxynitride layer.

The reason for using the nitride-based material for the hard mask insulation layer 83 is to provide an intended etch profile in the SAC process for forming the plug and simultaneously to prevent losses of the gate electrode patterns G1 and G2 because the nitride-based material has a different etch selectivity from an oxide-based inter-layer insulation layer.

Next, a nitride-based etch stop layer 84 is deposited thinly along a profile containing the gate electrode patterns G1 and G2. Then, a double insulation layer 85 including a first insulation layer 85A and a second insulation layer 85B is deposited on an entire surface of the above substrate structure. At this time, the double insulation layer 85 uses an oxide-based material. Also, the double insulation layer 85 is for insulating inter-layers and isolating the gate electrode patterns G1 and G2 from each other. The reason for forming the double insulation layer 85 is because a typically used insulation material, e.g., BPSG, has a poor adhesion with the photoresist pattern.

In more detail of the double insulation layer 85

deposition, the first insulation layer 85A made of BPSG is deposited on the entire substrate structure and is subsequently planarized. The second insulation layer 85B made of TEOS or HDP oxide is deposited thereon. The TEOS and the HDP oxide have a better adhesion with the photoresist pattern than the BPSG.

Referring to Fig. 6B, subsequent to the double insulation layer 85 deposition, a photoresist pattern 86, which is a cell contact open mask, is formed on the second insulation layer 85B. Then, the first and the second insulation layers 85A and 85B viewed in a direction of the line A-A' are selectively etched with use of the photoresist pattern 86 as an etch mask so that a plurality of opening parts 87 exposing substrate regions, e.g., impurity contact regions such like source/drains disposed between the gate electrode patterns G1 are formed in the cell region X-X'. On the other hand, the opening parts 87 viewed in a direction of the line B-B' expose the substrate regions disposed between the insulating patterns, i.e., the etched double insulation layer 85.

Next, a photoresist strip process is carried out to remove the photoresist pattern 86, and then, a cleaning process is performed to remove etch remnants and extend an opened portion of the opening part 87. At this time, compared to the single layer structure of the insulation layer, this double insulation layer 85 prevents an excessive etching of the insulation layer.

Referring to Fig. 6C, a plug conductive layer is deposited on the above entire structure so as to be electrically connected to the exposed substrate 80. Herein, the plug conductive layer is made of polysilicon or tungsten, and a barrier layer such as Ti/TiN can be formed at a bottom of the plug conductive layer. Afterwards, a CMP process is performed in such a manner that the second insulation layer 85B remains on an upper part of the gate electrode patterns G1 and G2 with a certain thickness. From this CMP process, a plurality of plugs 88 isolated from each other by the insulation layer 85 are formed.

Next, referring to Fig. 6D, the first and the second insulation layers 85A and 85B in the peripheral circuit region Y-Y' are removed through the use of a wet etching process. This removal of the double insulation layer 85 is denoted as the reference numeral 90. In more detail, a photoresist pattern 89 masking an upper part of the cell region X-X' is formed, and the first and the second insulation layers 85A and 85B in the peripheral circuit region Y-Y' are selectively removed by using the photoresist pattern 89 as an etch mask. Herein, such wet solution as BOE or HF is used in the wet etching process.

As described above, during the wet etching process, the wet solution is possibly diffused into interstitial spaces between the insulation layer and the photoresist pattern because of a poor adhesion of the typical insulation material, i.e., BPSG, with the photoresist. This diffused wet solution

results in defects in a semiconductor device. To solve this problem, three different methods are suggested in accordance with the present invention as the following:

First, as shown in the first preferred embodiment of the present invention, the dummy pattern is formed between the cell and the peripheral circuit regions when the plugs for cell contacts are formed.

Second, as shown in the second preferred embodiment of the present invention, the insulation layer is partially removed through the dry etching process having an anisotropic etching property, and then, the remaining insulation layer is removed through the wet etching process. As a result of the partial removal of the insulation layer, it is possible to shorten a period for performing the wet etching process, and thereby preventing the diffusions of the wet solutions.

Third, as shown in the third preferred embodiment of the present invention, the insulation layer is formed with double layers since the diffusions of the wet solution is also caused by a poor adhesion between the photoresist and the insulation layer typically made of BPSG. Instead of using merely the BPSG, such material as HDP oxide or TEOS having a good adhesiveness with the photoresist, is deposited on the BPSG layer to thereby prevent the diffusions of the wet solutions into the interstitial spaces between the photoresist pattern and the insulation layer.

In accordance with the first to the third preferred embodiment of the present invention, it is possible to prevent

deterioration of device characteristics resulted from the diffusions of the wet solution into the cell region during the removal of the insulation layer in the peripheral circuit region. With this prevention, it is ultimately possible to  
5 increase yields of the semiconductor device.

While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of  
10 the invention as defined in the following claims.